library ieee;

use ieee.std\_logic\_1164.all;

entity somador is port (

a, b, c : in std\_logic;

soma, carry: out std\_logic;

);

end somador;

architecture arch\_somador of somador is

component meio\_somador is port(

a, b: in std\_logic;

soma, carry: out std\_logic;

);

end component;

signal S\_primeira\_soma: std\_logic;

signal S\_primeiro\_carry: std\_logic;

signal S\_segundo\_carry: std\_logic;

begin

somador1: meio\_somador port map(

a => a,

b => b,

soma => S\_primeira\_soma,

carry => S\_primeiro\_carry

);

somador2: meio\_somador port map(

a => S\_primeira\_soma,

b => c,

soma => soma,

carry => S\_segundo\_carry

);

carry <= S\_primeiro\_carry or S\_segundo\_carry;

end arch\_somador;